Practitioner's Docket No. MI22-2536

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Fernando Gonzalez et al.

Application No.: 10/817,175
Filed: 03/31/04

Group No.: 2811
Examiner: Unassigned

For: **Methods of Forming Semiconductor Circuitry**

Commissioner for Patents
Washington, D.C. 20231

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being facsimile transmitted to the Patent and Trademark Office at (703) 872-9306 on the date shown below:

Facsimile Transmittal
Supplemental Information Disclosure Statement
PTO-Form 1449 and 2 cited article references

10/1/04
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Total Pages 11

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/817,175
Filing Date ..... March 31, 2004
Inventor ..... Fernando Gonzalez et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2811
Examiner ..... Unassigned
Attorney's Docket No. MI22-2536
Title: Methods of Forming Semiconductor Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. Copies of the cited art are included with the exception of U. S. patents and published U.S. applications (1276 Off. Gaz. Pat. Off., 05 August 2003). No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed before the mailing of a first Office Action, therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 9/30/04

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Form PTO-1449 — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
M22-2536	10/817,175
APPLICANT: Fernando Gonzalez et al.	
FILING DATE: 03/31/04	GROUP: 2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,903,108	02/90	Young et al.			
	AB	6,566,210 B2	05/03	Ajmera et al.			
	AC	5,650,343	07/97	Luning et al.			
	AD	6,306,691	10/01	Koh			
	AE	2001/0045604 A1	11/01	Oda et al.			
	AF	2001/0008292 A1	07/01	Loobandung et al.			
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Lee et al., "Investigation of poly-Si1-xGex for dual-gate CMOS Technology," IEEE Electron Device Letters, Vol. 19, No. 7, 1998, pgs. 247-249.
	AS		Wolf et al., "Silicon Processing for the VLSI Era Vol. 1 - Process Technology," Lattice Press, 1986, pgs. 191-194.
	AT		

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.